灰度科技
HUIDU TECHNOLOGY

Product specs

Receiving card R505

V3.0 20170901

Features

1. For the color screen, die-casting aluminum boxes and other lightweight structure design, standard interface;
2. Free external power supply design, through the adapter board to the card for power supply, increase hardware stability;
3. Inherit all the technical advantages and features of R500 series receiver card
4. With A60X, A30, A30 +, C30, C10 and other asynchronous sending card to use.

Main parameters

Working with sending card	Used in Sending card A60X、A30、A30+、C30、C10 etc.
Support modules	Used indoor, outdoor full color led displays, and single display； Support MBI5041/5042、MBI5050、MY9221、MY9268 etc. and PWM IC
Scan mode	Static and1-32 scan randomly
Communication distance	Gigabit Ethernet
One PCS Receiving card control range	256*192 (suggest) Max: 190,000 points, 1024 * 192
Receiving cards Connection settings	Receiving card set sequence randomly, and recognized automatically or by hand

Gray scale	0-65536
Smart setting	Smart setting of few simple steps by HDPlayer, and according to led module circuit board, it can smart setting too.
Play contents	Play video、animation、picture、text、3D text、 excel、PPT、time、counter etc.
Test functions	It have test button, and test modes of red、green、blue、white、gray、oblique line、 grid、spots etc.
Port	Normal terminal power supply or HUB board pin power supply (simplified box design), two Gigabit Ethernet ports, two 60PIN Universal Interface
Blanking circuit	Support
Communication distance	140meters by CAT5 or CAT6 LAN Cable
Voltage	4V-6V
Working temperature	-40℃-85℃

HUB signal details

1）16 RGB (default)

Table 2 60P PIN definition of normal mode

J1					J2			
1	C	A	2		1	C	A	2
3	B	OE	4		3	B	OE	4
5	LAT	CLK	6		5	LAT	CLK	6
7	D	E	8		7	D	E	8
9	R1a	G1	10		9	R9a	G9	10
11	R1b	B1	12		11	R9b	B9	12
13	GND	R2a	14		13	GND	R10a	14

15	G2	R2b	16		15	G10	R10b	16
17	B2	R3a	18		17	B10	R11a	18
19	G3	GND	20		19	G11	GND	20
21	R3b	B3	22		21	R11b	B11	22
23	R4a	G4	24		23	R12a	G12	24
25	R4b	B4	26		25	R12b	B12	26
27	NC	NC	28		27	NC	NC	28
29	NC	VCC	30		29	NC	VCC	30
31	C	A	32		31	C	A	32
33	B	OE	34		33	B	OE	34
35	LAT	CLK	36		35	LAT	CLK	36
37	D	E	38		37	D	E	38
39	R5a	G5	40		39	R13a	G13	40
41	R5b	B5	42		41	R13b	B13	42
43	GND	R6a	44		43	GND	R14a	44
45	G6	R6b	46		45	G14	R14b	46
47	B6	R7a	48		47	B14	R15a	48
49	G7	GND	50		49	G15	GND	50
51	R7b	B7	52		51	R15b	B15	52
53	R8a	G8	54		53	R16a	G16	54
55	R8b	B8	56		55	R16b	B16	56
57	NC	NC	58		57	NC	NC	58
59	NC	VCC	60		59	NC	VCC	60

Table2，A、B、OE、LAT、CLK、C、D、Ethe definition of these signals in the J1 ~ J2 is the same, that is, only need to FPGA pin number is 8PINs, and 16 groups Rxa, Gx, Rxb, Bx signal independent, need FPGA pin number 64PINs, a total of 8+ 64 = 72 PINs.

2）24GRB

Table 3 24P parallel data mode 60P pin definition

J1					J2			
1	C	A	2		1	C	A	2
3	B	OE	4		3	B	OE	4
5	LAT	CLK	6		5	LAT	CLK	6
7	D	E	8		7	D	E	8
9	F/SR	R1	10		9	F/SR	R13	10
11	G1	B1	12		11	G13	B13	12

13	GND	R2	14		13	GND	R14	14
15	G2	B2	16		15	G14	B14	16
17	R3	G3	18		17	R15	G15	18
19	B3	GND	20		19	B15	GND	20
21	R4	G4	22		21	R16	G16	22
23	B4	R5	24		23	B16	R17	24
25	G5	B5	26		25	G17	B17	26
27	R6	G6	28		27	R18	G18	28
29	B6	VCC	30		29	B18	VCC	30
31	C	A	32		31	C	A	32
33	B	OE	34		33	B	OE	34
35	LAT	CLK	36		35	LAT	CLK	36
37	D	E	38		37	D	E	38
39	F/SR	R7	40		39	F/SR	R19	40
41	G7	B7	42		41	G19	B19	42
43	GND	R8	44		43	GND	R20	44
45	G8	B8	46		45	G20	B20	46
47	R9	G9	48		47	R21	G21	48
49	B9	GND	50		49	B21	GND	50
51	R10	G10	52		51	R22	G22	52
53	B10	R11	54		53	B22	R23	54
55	G11	B11	56		55	G23	B23	56
57	R12	G12	58		57	R24	G24	58
59	B12	VCC	60		59	B24	VCC	60

Table 3, A, B, OE, LAT, CLK, C, D, E these signals in the definition of J1 ~ J2 is the same, that is, only need to FPGA pin number 8PINs, , Bx signal independent, need FPGA pin number is 72PINs, altogether needs 8 + 72 = 80PINs.

3）28GRB.

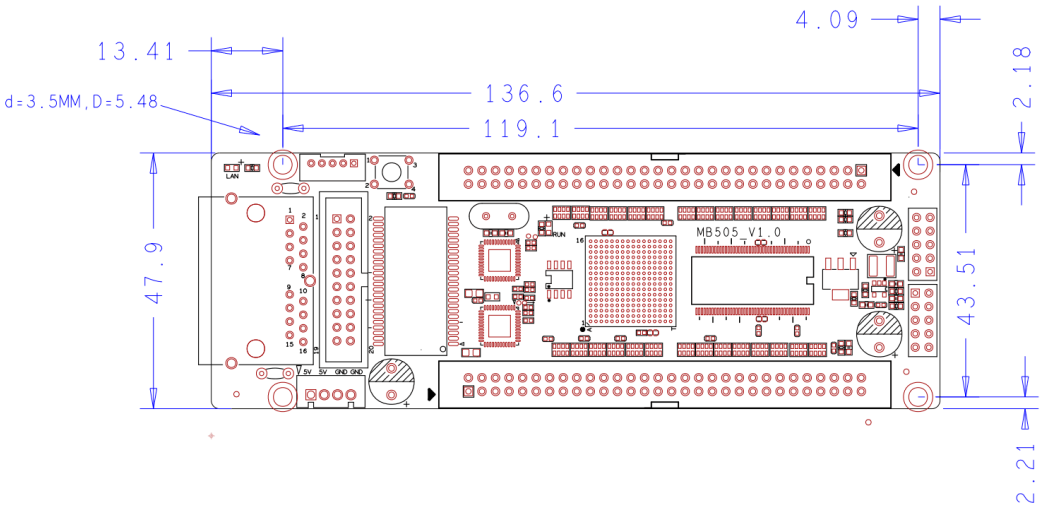
Table 4 Group 60P parallel data mode definition of the pin

J1					J2			
1	C	A	2		1	C	A	2
3	B	OE	4		3	B	OE	4
5	LAT	CLK	6		5	LAT	CLK	6
7	R1	G1	8		7	R15	G15	8
9	B1	R2	10		9	B15	R16	10
11	G2	B2	12		11	G16	B16	12

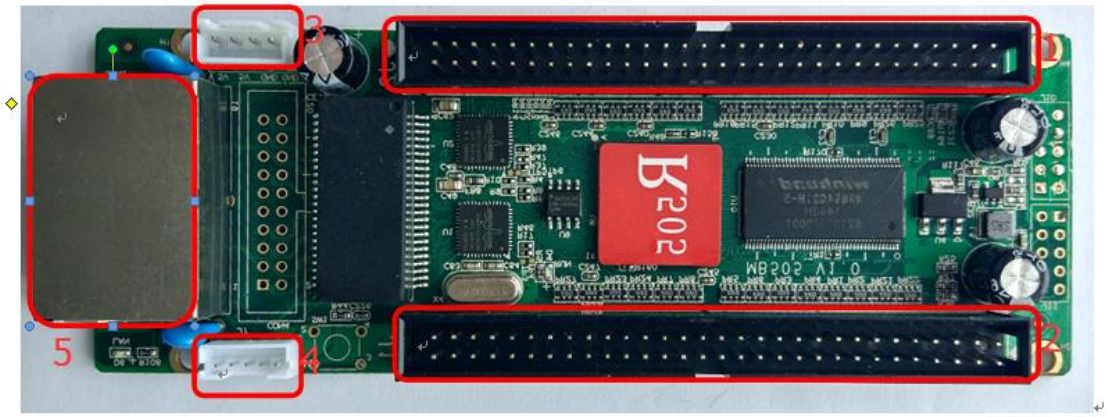
13	GND	R3	14		13	GND	R17	14
15	G3	B3	16		15	G17	B17	16
17	R4	G4	18		17	R18	G18	18
19	B4	GND	20		19	B18	GND	20
21	R5	G5	22		21	R19	G19	22
23	B5	R6	24		23	B19	R20	24
25	G6	B6	26		25	G20	B20	26
27	R7	G7	28		27	R21	G21	28
29	B7	VCC	30		29	B21	VCC	30
31	C	A	32		31	C	A	32
33	B	OE	34		33	B	OE	34
35	LAT	CLK	36		35	LAT	CLK	36
37	R8	G8	38		37	R22	G22	38
39	B8	R9	40		39	B22	R23	40
41	G9	B9	42		41	G23	B23	42
43	GND	R10	44		43	GND	R24	44
45	G10	B10	46		45	G24	B24	46
47	R11	G11	48		47	R25	G25	48
49	B11	GND	50		49	B25	GND	50
51	R12	G12	52		51	R26	G26	52
53	B12	R13	54		53	B26	R27	54
55	G13	B13	56		55	G27	B27	56
57	R14	G14	58		57	R28	G28	58
59	B14	VCC	60		59	B28	VCC	60

Table 4, A, B, C, OE, LAT, CLK several signals in the definition of J1 ~ J2 is the same, that is, only need to FPGA pins 6PINs, and 28 groups of Rx, Gx, Bx signal independent , Requires FPGA pin number 28 * 3 = 84PINs, a total of 6 +84 = 90PIN.

Assemble Photos



Appearance Description



①：1group 2X30PIN standard output interface，connect the LED screen.

②：1group 2X30PIN standard output interface，connect the LED screen.

③：：Indicator interface.

④：Power interface can be accessed 5V voltage;

⑤：Gigabit Ethernet port.

Technical Parameters

	Minimum	Typical value	Maximum
Rated voltage (V)	4.2	5.0	5.5
Storage temperature(℃)	-40	25	105
Work environment humidity (℃)	-40	25	80
Work environment humidity (%)	0.0	30	95

Precaution

1）In order to ensure the long-term stable operation of the system; please try to use the standard 5V power supply voltage.